SHARP

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To : _____

PRELIMINARY

SPECIFICATIONS

Product Type 1/1-type Progressive Scan Color CCD Area Sensor with 6M Pixels (4ch)

Model No R J 3 D T 3 A F 0 D T

※ This specifications contains 24 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE : _____

BY : _____

PRESENTED

BY : J. Nakai

J.NAKAI
Dept. General Manager

REVIEWED BY : T. Yoshida

PREPARED BY : Y. Nakashima

Development Dept. VI
Sensing Device Division
Electronic Components And Devices Division
SHARP CORPORATION

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- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc

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- Aerospace equipment
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- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

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○ Please direct all queries and regarding the products covered herein to a sales representative of the company.

CONTENTS

RJ3DT3AF0DT

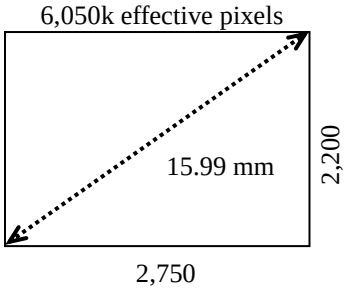
1/1-type Progressive Scan Color CCD Area Sensor with 6M Pixels (4ch)

1 DESCRIPTION

The RJ3DT3AF0DT is a 1/1-type solid-state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices, 4ch). With approximately 6,287k pixels, the sensor provides a high resolution stable color image.

1 . 1 Features

1) Optical size : 15.99 mm (Aspect ratio 4:3)
2) Progressive scan format
3) Square pixel
4) Number of total pixels : Horizontal 2832 × vertical 2220
   Number of image pixels : Horizontal 2758 × vertical 2208
   Number of effective pixels : Horizontal 2750 × vertical 2200
   Pixel pitch : Horizontal 4.54 μm × vertical 4.54 μm
   Number of optical black pixels : Horizontal ; 37 front (per channel)
   : Vertical ; 6 front (per channel)
   Number of dummy bits : Horizontal ; 4 front (per channel) , Vertical ; 2 front (per channel)
5) R, G and B primary color mosaic filters
6) Built-in overflow drain voltage output circuit, and reset gate voltage circuit
7) Variable electronic shutter
8) Low fixed pattern noise and lag
9) No burn-in and no image distortion
10) Blooming suppression structure
11) Built-in output amplifier
12) N-type silicon substrate, N-MOS process,
    Not designed or rated as radiation hardened
13) Global shutter



1 . 2 Applications

1) Industrial monitor cameras
2) Intelligent Transport Systems cameras
3) Video capturing devices for PCs, etc

iSHCCD Ⅱ in iSHartina

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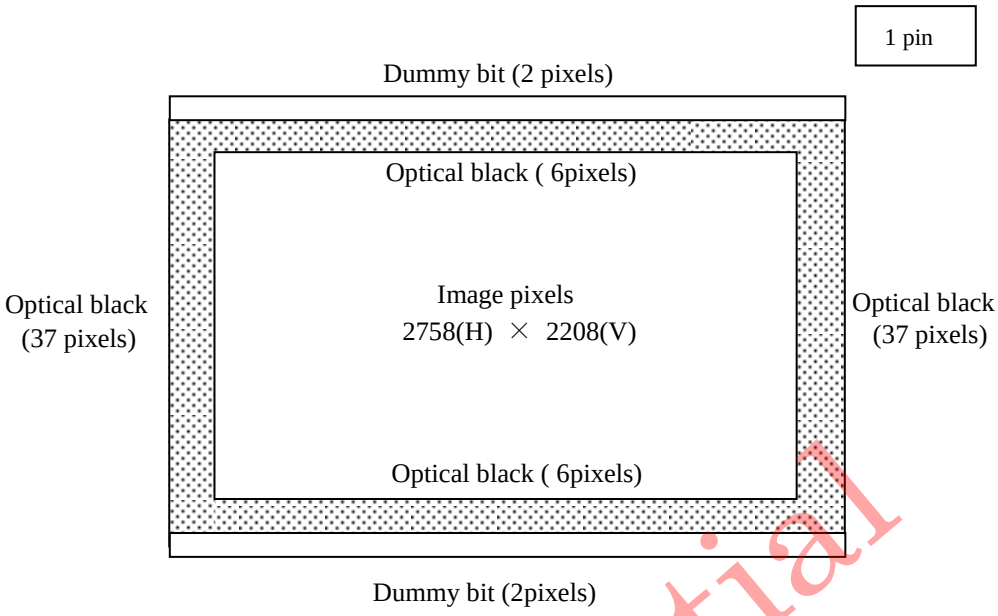
The "iSHCCD Ⅱ" is an advanced CCD image sensor that drastically improves light efficiency by including near-infrared light region as a basic structure of "iSHCCD".
The "iSHartina" series is a key device group of Sharp which realizes a next-generation sensing world.

The circuit diagram and others included in this specifications are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

2 ARRANGEMENT OF PIXELS AND COLOR FILTERS



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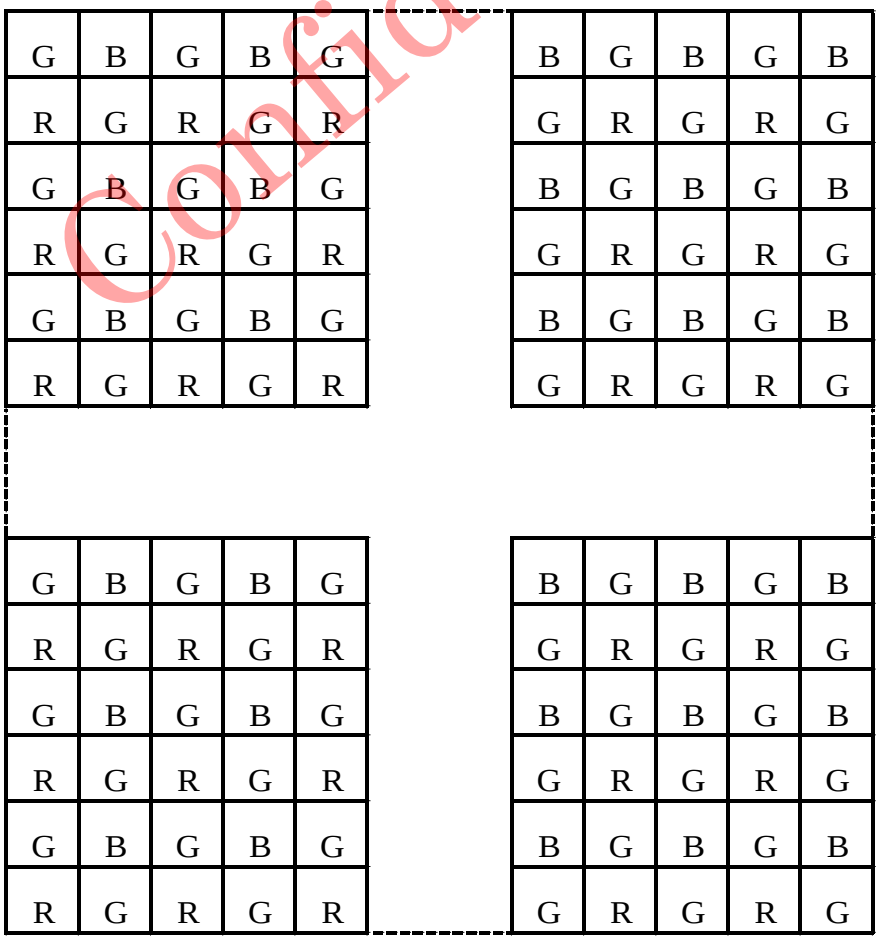
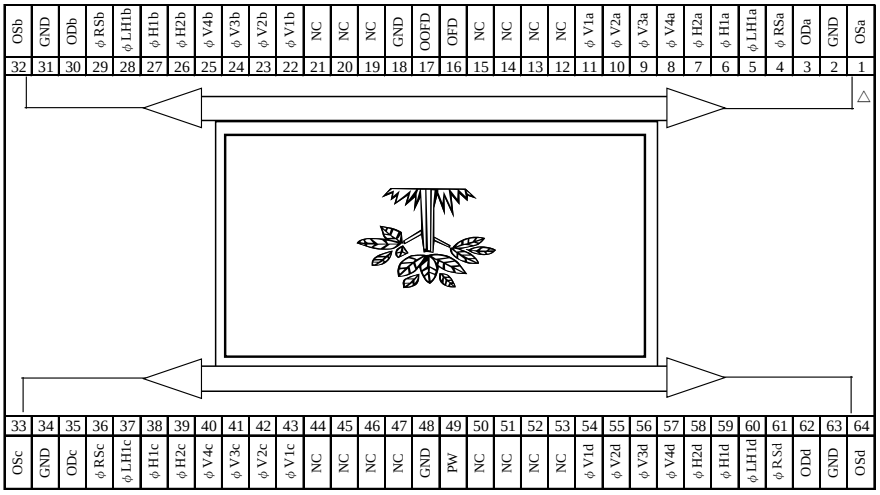


(1, 1) (2758, 1)

3 PIN CONFIGURATION(TOP VIEW)



Symbol	Pin name
ODa,ODb,ODc,ODd	Output transistor drain
OSa,OSb,OSc,OSd	Output signals
ϕ_{RSa}, ϕ_{RSb}, ϕ_{RSc}, ϕ_{RSd}	Reset transistor clock
ϕ_{V1a}, ϕ_{V1b}, ϕ_{V1c}, ϕ_{V1d}, ϕ_{V2a}, ϕ_{V2b}, ϕ_{V2c}, ϕ_{V2d}, ϕ_{V3a}, ϕ_{V3b}, ϕ_{V3c}, ϕ_{V3d}, ϕ_{V4a}, ϕ_{V4b}, ϕ_{V4c}, ϕ_{V4d}	Vertical shift register clock
ϕ_{LH1a}, ϕ_{LH1b}, ϕ_{LH1c}, ϕ_{LH1d}, ϕ_{H1a}, ϕ_{H1b}, ϕ_{H1c}, ϕ_{H1d}, ϕ_{H2a}, ϕ_{H2b}, ϕ_{H2c}, ϕ_{H2d}	Horizontal shift register clock
OFD	Overflow drain
OOFD	Output overflow drain
PW	P_well
GND	Ground

4 ABSOLUTE MAXIMUM RATINGS

(T_A=25℃)

Parameter	Symbol	Ratings	Unit
Output transistor drain voltage	V_{OD}	0 to +15.4	V
Overflow drain voltage	V_{OFD}	0 to +32	V
Overflow drain output voltage	V_{OOFD}	Internal output (Note 1)	
Reset gate clock voltage	$V_{\phi RS}$	Internal output (Note 2)	
Vertical shift register clock voltage	$V_{\phi V}$	V_{PW} to +15.4	V
Horizontal shift register clock voltage	$V_{\phi H}$	-0.3 to +5.1	V
Voltage difference between P_well and vertical clock	V_{PW}-$V_{\phi V}$	-23.8 to +0	V
Voltage difference between vertical clocks	$V_{\phi V}$-$V_{\phi V}$	0 to +9.9 (Note 3)	V
Storage temperature	T_{STG}	-40 to +90	℃
Ambient operating temperature	T_{OPR}	-30 to +85	℃

(Note 1) Use the circuit parameter indicated in "8. EXAMPLE OF STANDARD OPERATING CIRCUIT" and do not connect to DC voltage directly. When OOFD is connected to GND, connect V_{OD} to GND.

(Note 2) Do not connect to DC voltage directly. When ϕ_{RS} is connected to GND, connect V_{OD} to GND. Reset gate clock is applied below 5.1 Vp-p.

(Note 3) When clock width is below 10 μs, and clock duty factor is below 0.1 %, voltage difference between adjoining vertical clocks are guaranteed up to 15.4 V.
Do not change all ϕ_V during 0.5 μs before rising edge of $V_{\phi VH}$ pulse and after falling edge of $V_{\phi VH}$ pulse.
Do not change directly into $V_{\phi VL} \rightarrow V_{\phi VH}$ or $V_{\phi VH} \rightarrow V_{\phi VL}$.

5 RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Ambient operating temperature		T_{OPR}		25.0		℃
Output transistor drain voltage		V_{ODa},V_{ODb},V_{ODc},V_{ODd}	13.1	13.5	13.9	V
Overflow drain clock	p-p level (Note 1)	$V_{\phi OFD}$	19.3	20.0	20.7	V
Ground		GND		0.0		V
P_well voltage	(Note 2)	V_{PW}	-6.8		$V_{\phi VL}$	V
Vertical shift register clock	LOW level	$V_{\phi V1aL}$,$V_{\phi V1bL}$,$V_{\phi V1cL}$,$V_{\phi V1dL}$, $V_{\phi V2aL}$,$V_{\phi V2bL}$,$V_{\phi V2cL}$,$V_{\phi V2dL}$, $V_{\phi V3aL}$,$V_{\phi V3bL}$,$V_{\phi V3cL}$,$V_{\phi V3dL}$, $V_{\phi V4aL}$,$V_{\phi V4bL}$,$V_{\phi V4cL}$,$V_{\phi V4dL}$	-6.8	-6.5	-6.2	V
	INTERMEDIATE level	$V_{\phi V1aI}$,$V_{\phi V1bI}$,$V_{\phi V1cI}$,$V_{\phi V1dI}$, $V_{\phi V2aI}$,$V_{\phi V2bI}$,$V_{\phi V2cI}$,$V_{\phi V2dI}$, $V_{\phi V3aI}$,$V_{\phi V3bI}$,$V_{\phi V3cI}$,$V_{\phi V3dI}$, $V_{\phi V4aI}$,$V_{\phi V4bI}$,$V_{\phi V4cI}$,$V_{\phi V4dI}$		0.0		V
	HIGH level	$V_{\phi V1aH}$,$V_{\phi V1bH}$,$V_{\phi V1cH}$,$V_{\phi V1dH}$	13.1	13.5	13.9	V
Horizontal shift register clock	LOW level	$V_{\phi LH1aL}$, $V_{\phi LH1bL}$, $V_{\phi LH1cL}$, $V_{\phi LH1dL}$, $V_{\phi H1aL}$,$V_{\phi H1bL}$, $V_{\phi H1cL}$,$V_{\phi H1dL}$, $V_{\phi H2aL}$, $V_{\phi H2bL}$, $V_{\phi H2cL}$, $V_{\phi H2dL}$	-0.05	0.0	0.05	V
	HIGH level	$V_{\phi LH1aH}$, $V_{\phi LH1bH}$, $V_{\phi LH1cH}$,$V_{\phi LH1dH}$, $V_{\phi H1aH}$,$V_{\phi H1bH}$, $V_{\phi H1cH}$,$V_{\phi H1dH}$, $V_{\phi H2aH}$,$V_{\phi H2bH}$, $V_{\phi H2cH}$,$V_{\phi H2dH}$	3.15		3.6	V
Reset gate clock	p-p level (Note 1)	$V_{\phi RSa}$,$V_{\phi RSb}$,$V_{\phi RSc}$,$V_{\phi RSd}$	3.15		3.6	V
Vertical shift register clock frequency (Note 3)		$f_{\phi V1a}$,$f_{\phi V1b}$,$f_{\phi V1c}$,$f_{\phi V1d}$, $f_{\phi V2a}$,$f_{\phi V2b}$,$f_{\phi V2c}$,$f_{\phi V2d}$, $f_{\phi V3a}$,$f_{\phi V3b}$,$f_{\phi V3c}$,$f_{\phi V3d}$, $f_{\phi V4a}$,$f_{\phi V4b}$,$f_{\phi V4c}$,$f_{\phi V4d}$		35.1		KHz
Horizontal shift register clock frequency		f_{LH1a},f_{LH1b},f_{LH1c},f_{LH1d}, f_{H1a},f_{H1b},f_{H1c},f_{H1d}, f_{H2a},f_{H2b},f_{H2c},f_{H2d}		60.0		MHz
Reset gate clock frequency		$f_{\phi RSa}$,$f_{\phi RSb}$,$f_{\phi RSc}$,$f_{\phi RSd}$		60.0		MHz

（Note 1） Use the circuit parameter indicated in “EXAMPLE OF STANDARD OPERATING CIRCUIT”, and do not connect to DC voltage directly.

（Note 2） V_{PW} is set below $V_{\phi VL}$ that is low level of vertical shift register clock, or is used with the same power supply that is connected to V_L of V driver IC.

（Note 3） At frame accumulation mode.

※ To apply power, first connect GND and then turn on V_{OD}. After turning on V_{OD}, turn on V_{PW} first and then turn on other powers and pulses.
Do not connect the device to or disconnect it from the plug socket while power is being applied.

6 CHARACTERISTICS (Drive method：1/30s frame accumulation)

T_A：+25℃, but +60℃ for parameter No.4 and No.5.
Operating conditions：the typical values specified in “5 RECOMMENDED OPERATING CONDITIONS”.
Color temperature of light source：3200K, IR cut-off filter (CM-500,1 mm) is used.

No.	Parameter	Symbol	Note	Minimum	Typical	Maximum	Unit
1	Standard output voltage	V_O	1		150		mV
2	Photo response non-uniformity	PRNU	2			10	%
3	Saturation output voltage	V_{SAT}	3	1000			mV
4	Dark output voltage	V_{DARK}	4		0.5	3.0	mV
5	Dark signal non-uniformity	DSNU	5		0.5	2.0	mV
6	Sensitivity (Green channel)	R(G)	6	920	1150		mV
7	Smear ratio	SMR	7		-125	-110	dB
8	Image lag	AI	8			1.0	%
9	Blooming suppression ratio	ABL	9	1000			
10	Output transistor drain current	I_{OD}			24.0		mA

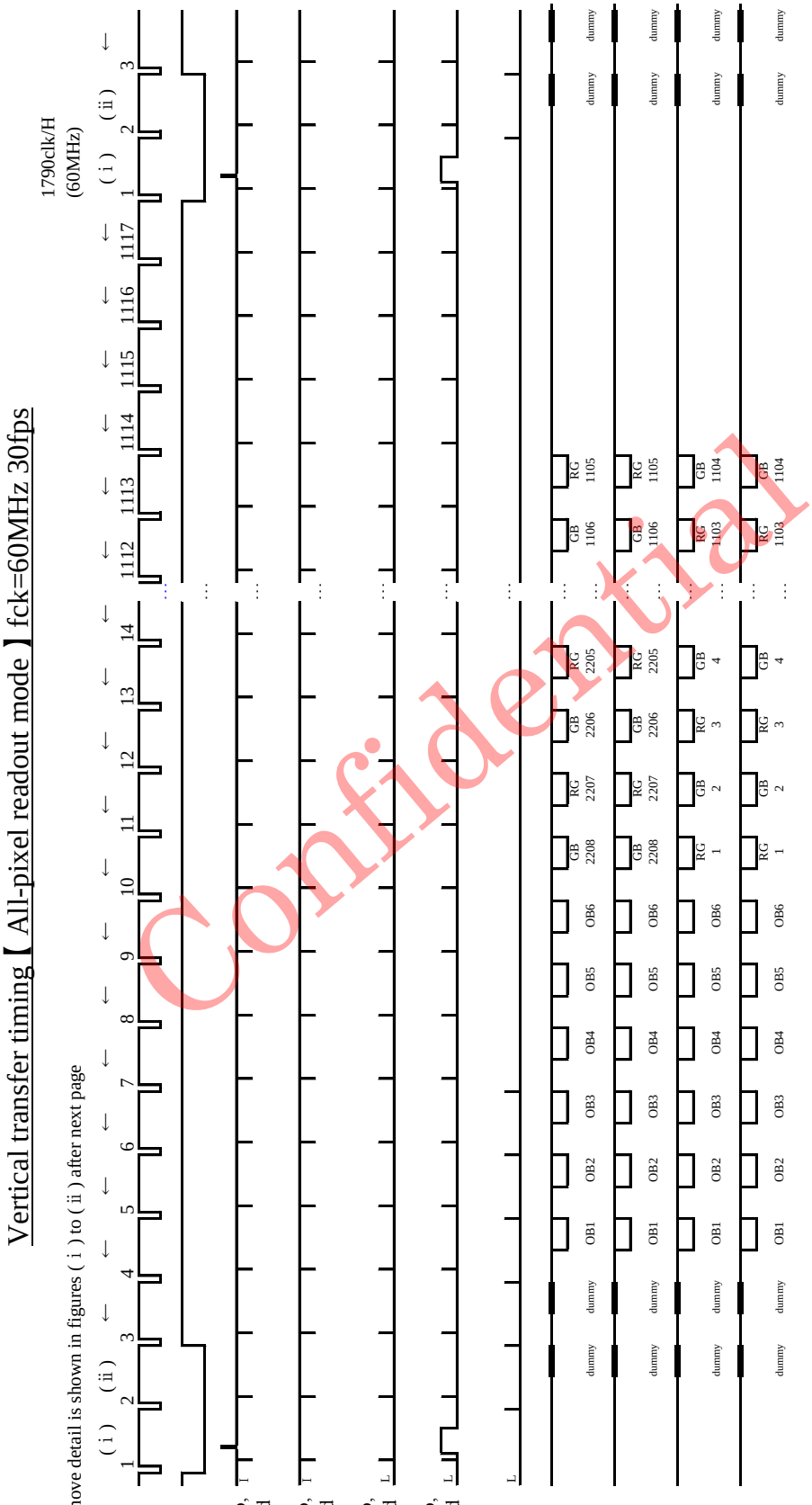
【 Notes 】

1 The average output voltage of G signal under the uniform illumination. The standard exposure conditions are defined as when V_O is 150 mV.
2 The image area is divided into 10 × 10 segments under the standard exposure conditions. Each segment’s voltage is the average output voltage of all pixels within the segment. PRNU is defined by (Vmax – Vmin) / V_O, where Vmax and Vmin are the maximum and minimum values of each segment’s voltage respectively.
3 The image area is divided into 10 × 10 segments. Each segment’s voltage is the average output voltages of all pixels within the segment. Vsat is the minimum segment’s voltage under 15 times exposure of the standard exposure conditions.
4 The average output voltage under non-exposure conditions.
5 The image area is divided into 10 × 10 segments under non-exposure conditions. DSNU is defined by (Vdmax – Vdmin), where Vdmax and Vdmin are the maximum and minimum values of each segment’s voltage respectively.
6 The average output voltage of G signal when a 1000 lux light source with a 90 % reflector is imaged by a lens of F4, f50 mm.
7 The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum output voltage in the V/10 square.
8 The sensor is exposed at the exposure level corresponding to the standard conditions. AI is defined by the ratio of the output voltage measured at the 1st field during the non-exposure period to the standard output voltage.
9 The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is defined by the ratio of the exposure at the standard conditions to the exposure at a point where blooming is observed.

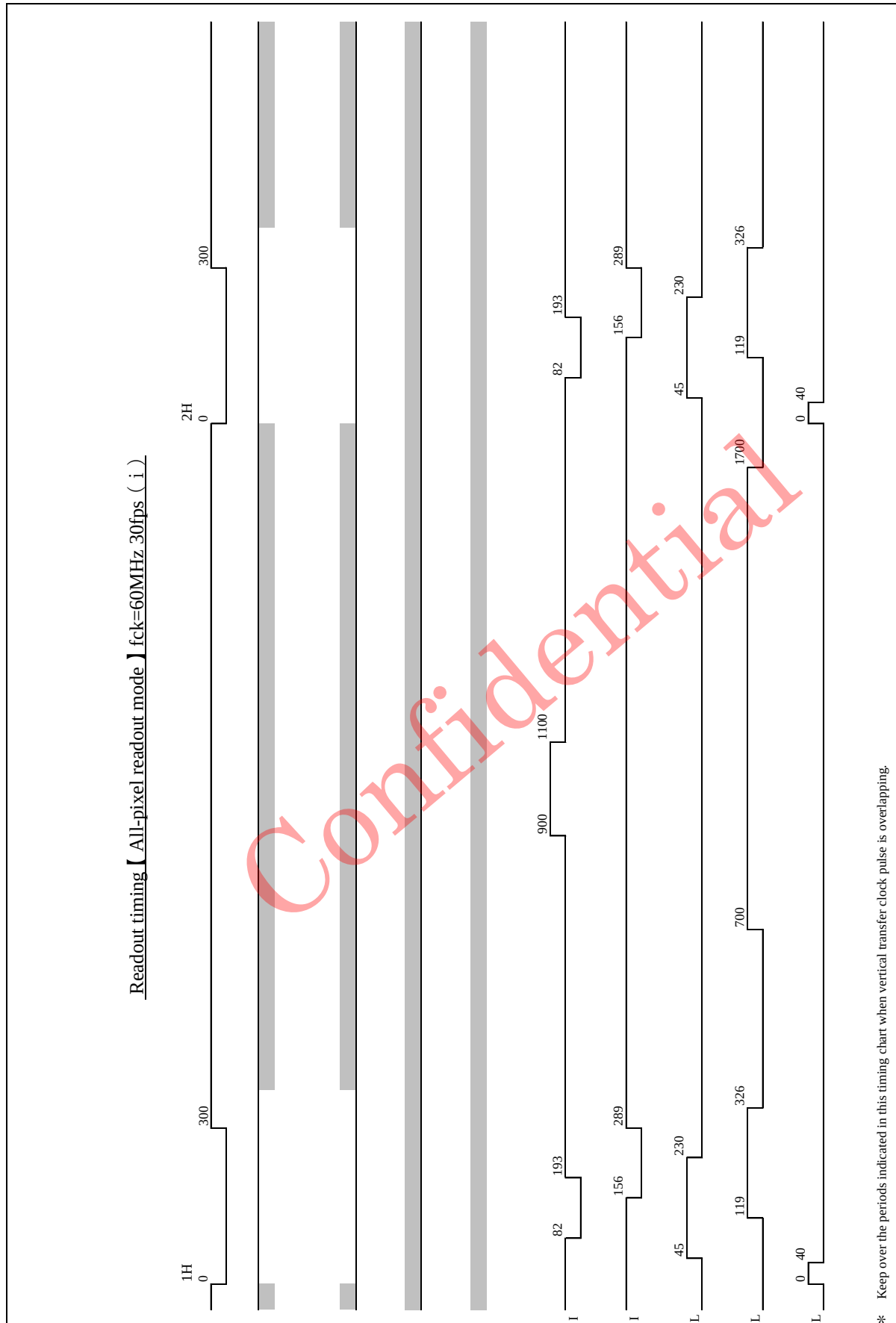
【 Comment 】

Within the recommended operating conditions of V_{OD}, V_{OFD} of the internal output satisfies with ABL and V_{SAT}.

7 DRIVE TIMING CHART

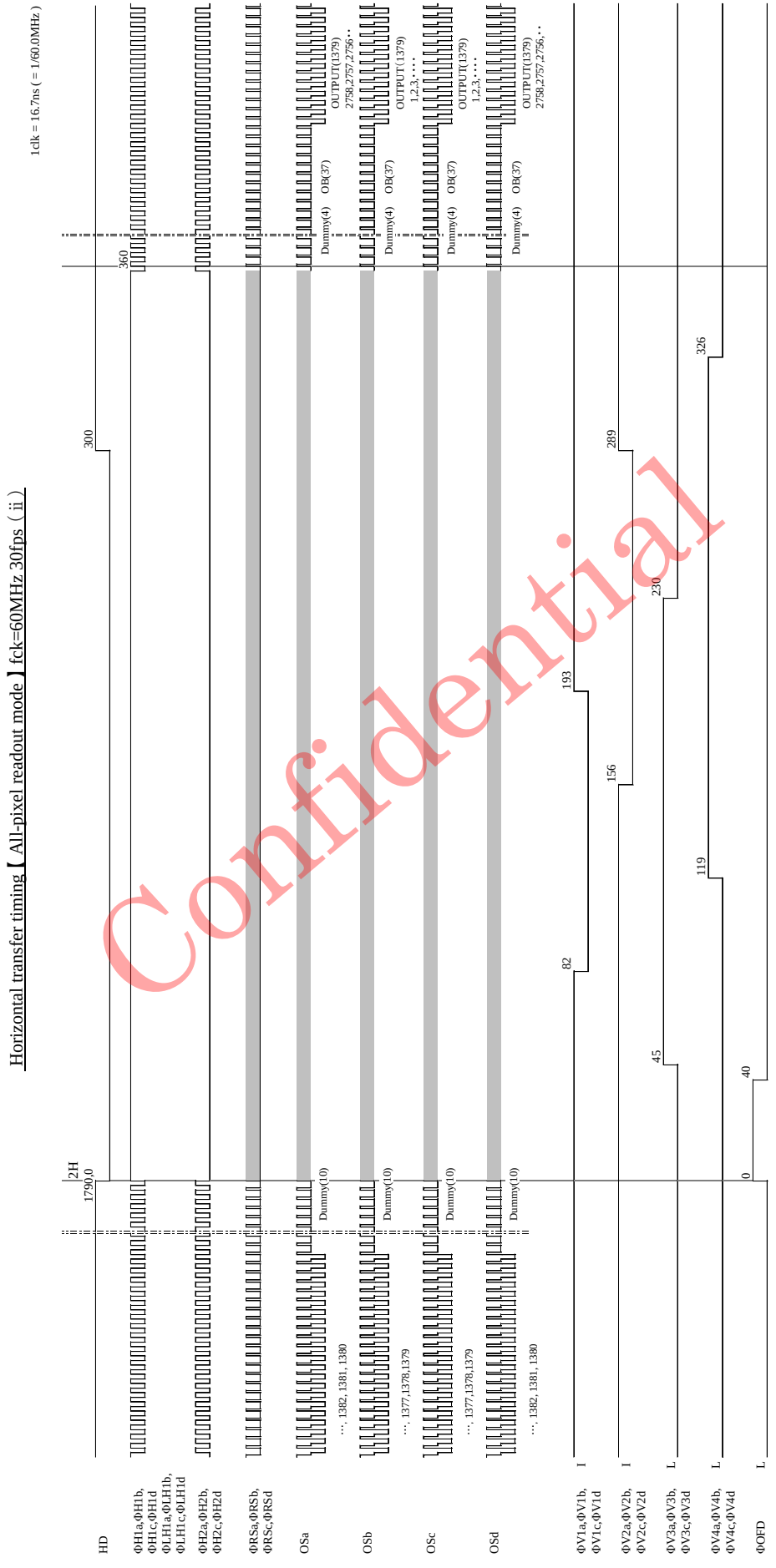


Readout timing【All-pixel readout mode】fck=60MHz 30fps（i）



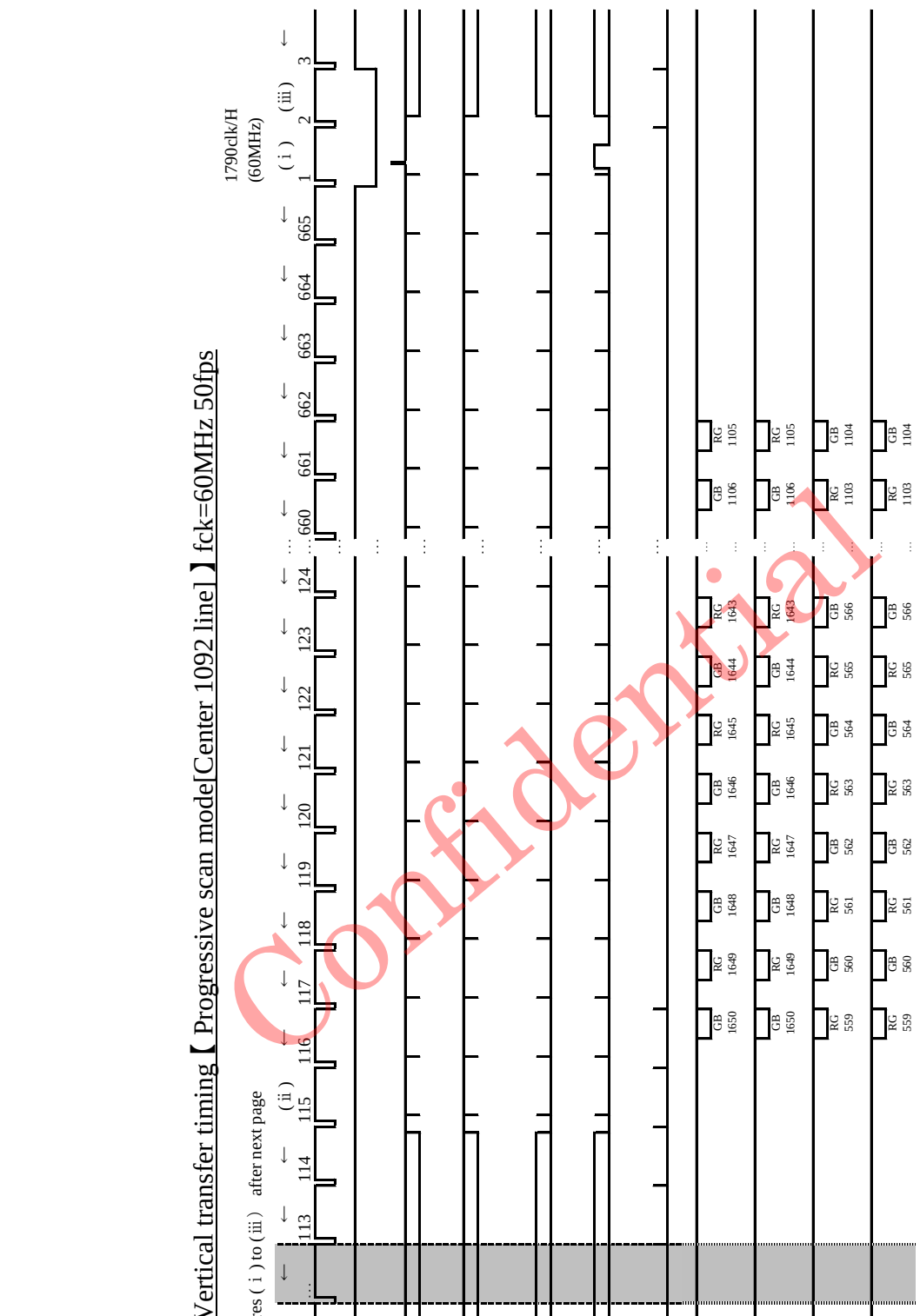
＊ Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Horizontal transfer timing【All-pixel readout mode】fck=60MHz 30fps（ii）

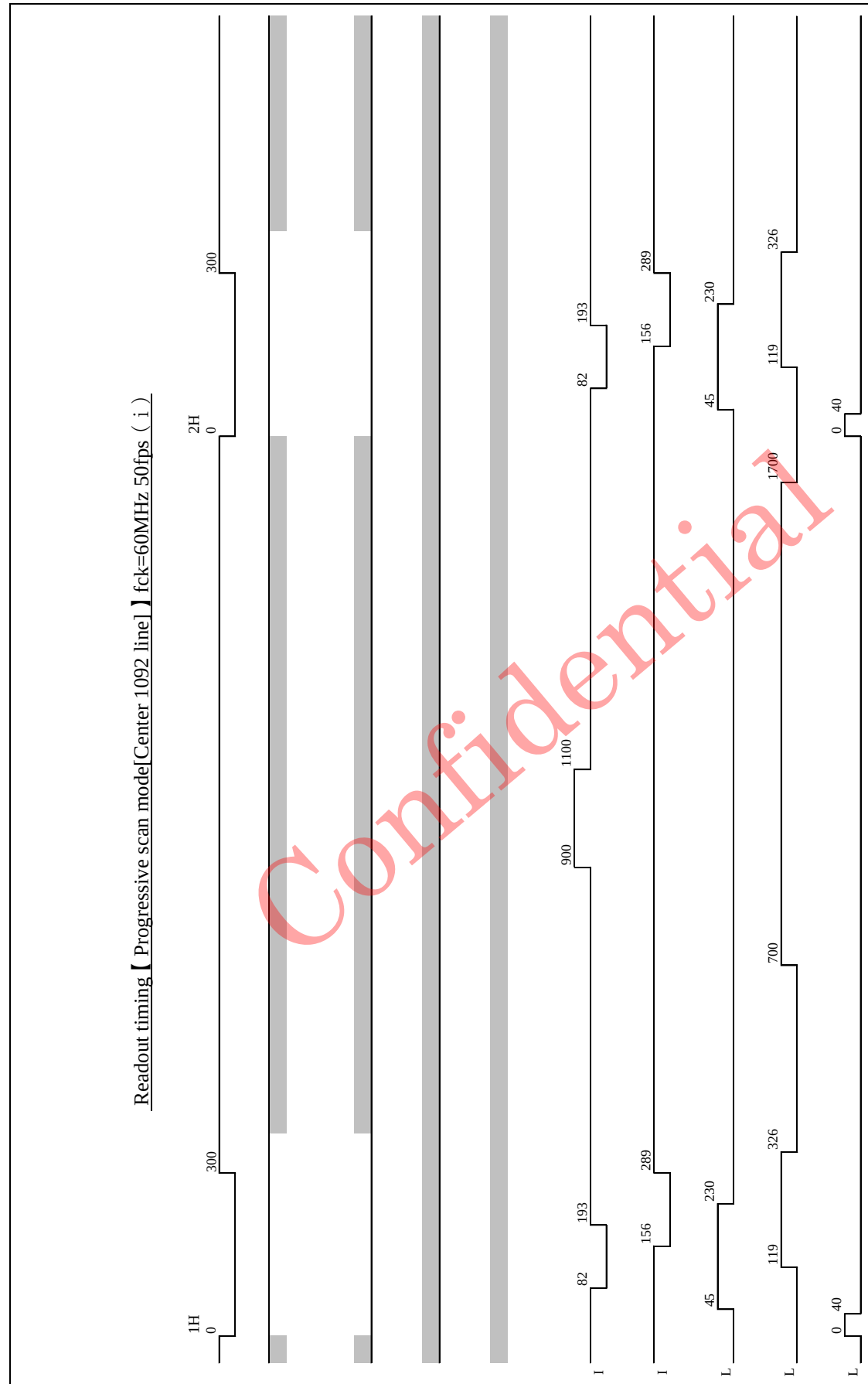


* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Vertical transfer timing 【Progressive scan mode[Center 1092 line]】 fck=60MHz 50fps

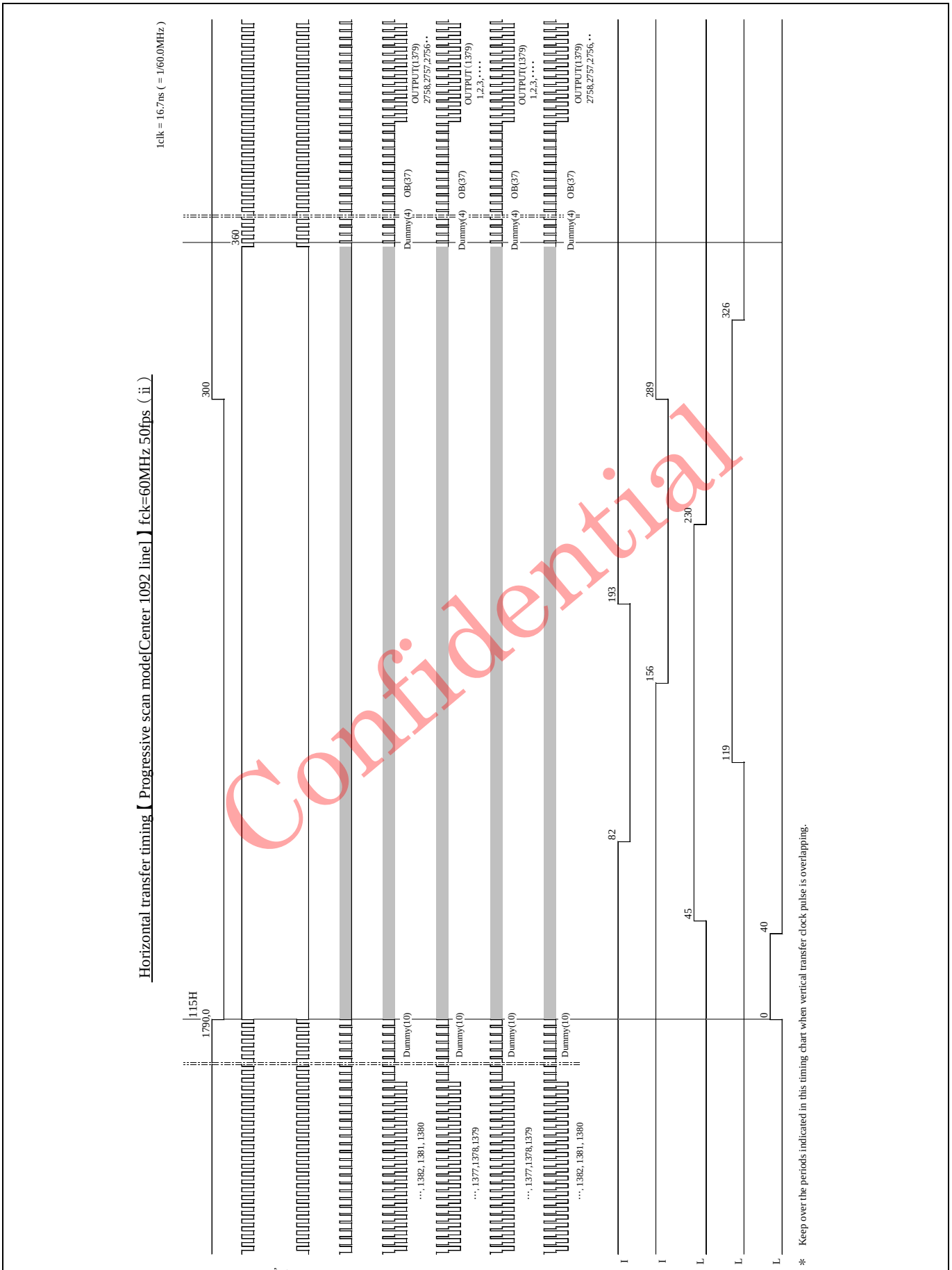


Readout timing【Progressive scan mode[Center 1092 line】fck=60MHz 50fps（i）



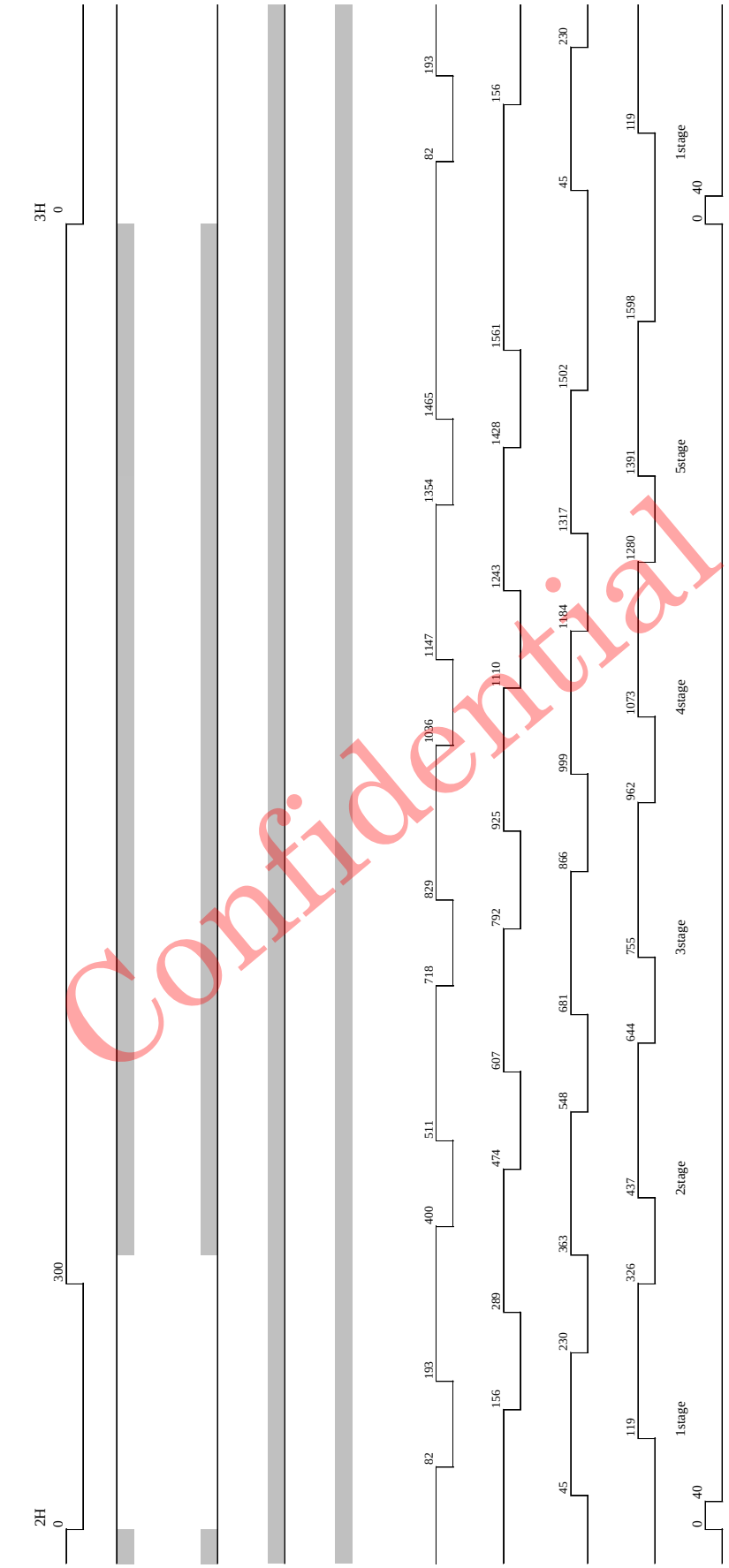
＊ Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Horizontal transfer timing【Progressive scan mode(Center 1092 line)】fck=60MHz 50fps（ii）



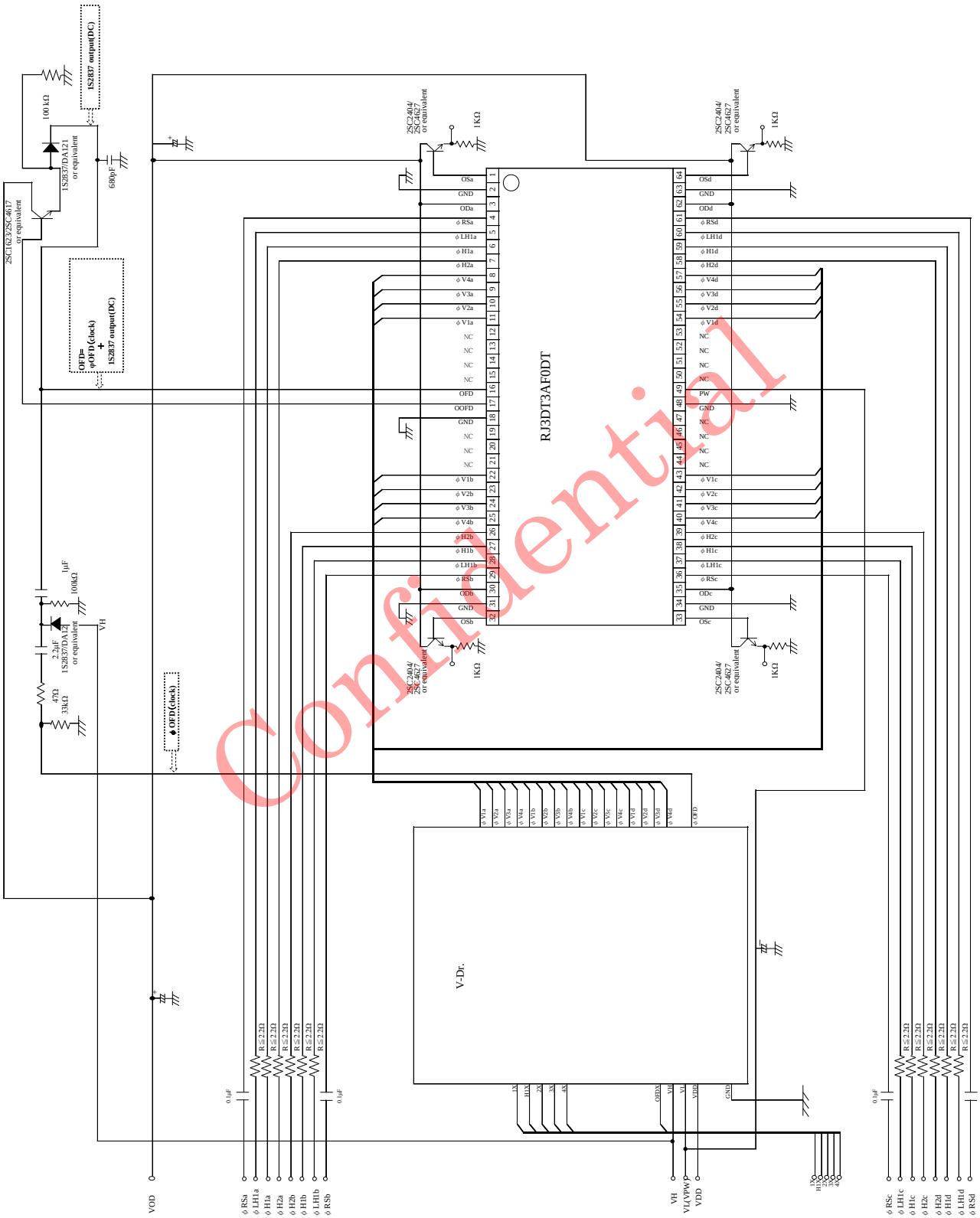
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

Fast shift transfer timing【Progressive scan mode(Center 1092 line)】fck=60MHz 50fps（iii）



* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.

8 EXAMPLE OF STANDARD OPERATING CIRCUIT



9 SPECIFICATION FOR BLEMISH (1/30 s frame accumulation)

1) Definition of blemish

	Level of blemish (mV)	Permitted number of blemish	Comment
White blemish (Exposed)	100≦ B	1	・See fig.9-1(a), fig.9-2. ・Vout = Vstd
	B ＜100	no count	
Black blemish (Exposed)	120≦ B	1	
	55≦ B ＜120	15	
	40≦ B ＜ 55	15	
	B ＜ 40	no count	
White blemish (Non-Exposed)	100＜ B	1	・See fig.9-1(b), fig.9-2 ・N≦150 ・M＋N≦750
	20＜ B ≦100	N	
	2.5＜ B ≦ 20	M	
	B ≦2.5	no count	
White blemish (Shutter mode)	5.0≦ B	0	・See fig.9-1(a), fig.9-2. ・Vout = Vstd/10 ・The electronic shutter speed is set at 1/10000 s
	B ＜5.0	no count	
Black blemish (Shutter mode)	5.0≦ B	0	
	B ＜5.0	no count	

・ B : Blemish level defined in fig. 9-1.
・ Vout : Average output voltage
・ Vstd : 150 mV (The average output voltage of G signal). The standard output voltage defined in the specification of the characteristics.

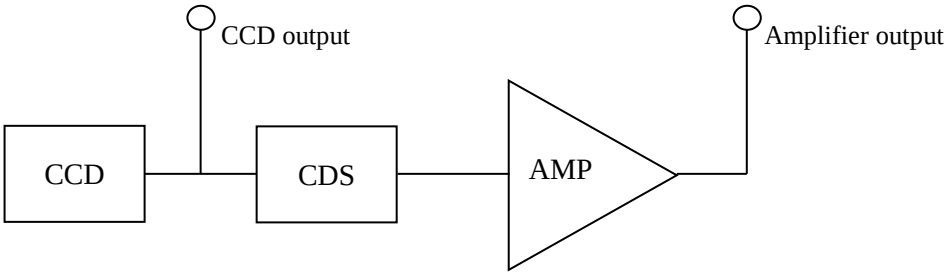
＊Total number of white blemish (non-exposed:20＜B) and black blemish (exposed:55≦B)are less than 2 in arbitrary 8×8 pixels areas(ignore color filter).

ex. The defects are less than 2 in the subsequent area surrounded by bold lines.

G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G	R	G

【MEASURING CONDITION】

・Ta： 60 ℃
・Measuring block diagram



The output voltage is measured at the CCD output.
The gain of the amplifier is adjusted to the unity between the CCD output and the amplifier output.

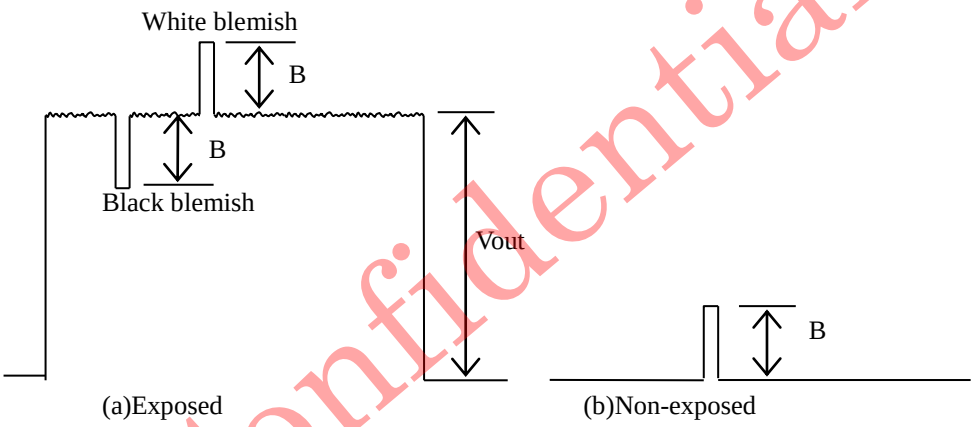


fig. 9-1 Definition of blemish level

(The wave form is the luminance signal measured at the Amplifier output)

【MEASURING AREA】

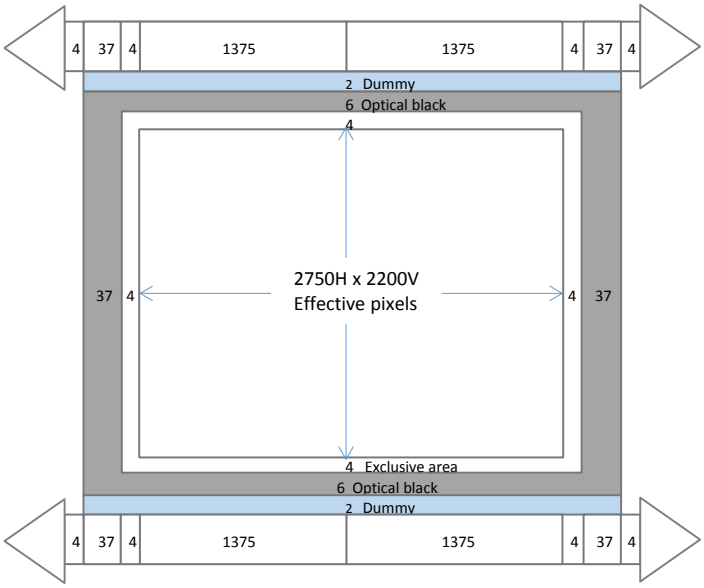


fig. 9-2 Definition of the measuring area

10 PRECAUTIONS

10.1 Package Breakage

In order to prevent the package from being broken, observe the following instructions:

1) The CCD is a precise optical component and the package material is plastic.
Therefore,
- Take care not to drop the device when mounting, handling, or transporting.
- Avoid giving a shock to the package. Especially when leads are fixed to the socket or the circuit board, small shock could break the package more easily than when the package isn't fixed.

2) When mounting the package on the housing, be sure that the package is not bent.
- If a bent package is forced into place between a hard plate or the like, the package may be broken.

3) If any damage or breakage occurs on the surface of the glass cap, its characteristics could deteriorate.
Therefore,
- Do not hit the glass cap.
- Do not give a shock large enough to cause distortion.
- Do not scrub or scratch the glass surface.
- Even a soft cloth or applicator, if dry, could cause flaws to scratch the glass.

10.2 Electrostatic Damage

As compared with general MOS-LSI, CCD has lower ESD.
Therefore, take the following antistatic measures when handling the CCD:

1) Always discharge static electricity by grounding the human body and the instrument to be used.
To ground the human body, provide resistance of about 1 MΩ between the human body and the ground to be on the safe side.
2) When directly handling the device with the fingers, hold the part without leads and do not touch any lead.
3) To avoid generating static electricity,
a. do not scrub the glass surface with cloth or plastic
b. do not attach any tape or labels
c. do not clean the glass surface with dust-cleaning tape
4) When storing or transporting the device, put it in a container of conductive material.

10.3 Dust and Contamination

Dust or contamination on the glass surface could deteriorate the output characteristics or cause a scar.
In order to minimize dust or contamination on the glass surface, take the following precautions:

1) Handle the CCD in a clean environment such as a cleaned booth. (The cleanliness level should be, if possible, class 1,000 at least.)

2) Do not touch the glass surface with the fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:

- Dust from static electricity should be blown off with an ionized air blower.
  For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.

- The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.

— Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note: In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommend that the above procedures should be taken to wipe out dust and contamination before using the device.

10.4 Other

1) Soldering should be manually performed within 5 seconds at 350℃ maximum at the tip of soldering iron.

2) Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.

3) CCD has the possibility that white blemish, which originates in the structure of CCD with the passage of time by an external factor such as the radiations, could be generated.
Please use white blemish compensation circuit for white blemish generated afterward.

4) Do not expose the device to strong light. For the color device, long exposure to strong light will fade the color of the color filters.

11. PACKAGE OUTLINE AND PACKING SPECIFICATION

1. Package Outline Specification

Refer to attached drawing.

（The seal resin stick out from the package shall be passed.）

2. Markings

Marking contents

（1）. Product name : RJ3DT3AF0DT

（2）. Company name : ＳＨＡＲＰ

（3）. Country of origin : ＪＡＰＡＮ

（4）. Date code : ＹＹ ＷＷ Ｘ ＸＸ

Denotes the production ref.code.(1～2 figures)

Denotes the production day of the week.

1	2	3	4	5	6	7
SUN.	MON.	TUE.	WED.	THU.	FRI.	SAT.

Denotes the production week.
（01,02,03,･･･,52,53）

Denotes the production year.
(Lower two digits of the year.)

Positions of markings are shown in the package outline drawing.
But,markings shown in that drawing are not provided any measurements of their characters and their positions.

3. Packing Specification

3－1. Packing materials

Material Name	Material Spec.	Purpose
Cover Tape	Plastic film(1device/tape)	Glass lid covering
Device case	Cardboard(126devices/case)	Device tray fixing
Device tray	Conductive plastic (21devices/tray)	Device packing(6trays/case)
Cover tray	Conductive plastic(1tray/case)	Device packing
PP band	Polypropylene	Device tray fixing
Buffer	Cardboard(2sheets/case)	Shock absorber of device tray
Plastic film bag	Plastic film	Device tray fixing
Tape	Paper	Sealing plastic film bag and device case
Label	Paper	Indicates part number,quantity and date of manufacture

3－2. External appearance of packing

Refer to attached drawing

4. Precaution

1）. Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specification.

2）. Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operator's body, too.

5. Chemical substance information in the product

Product Information Notification based on Chinese law, Management Methods for Controlling Pollution by Electronic Information Products.

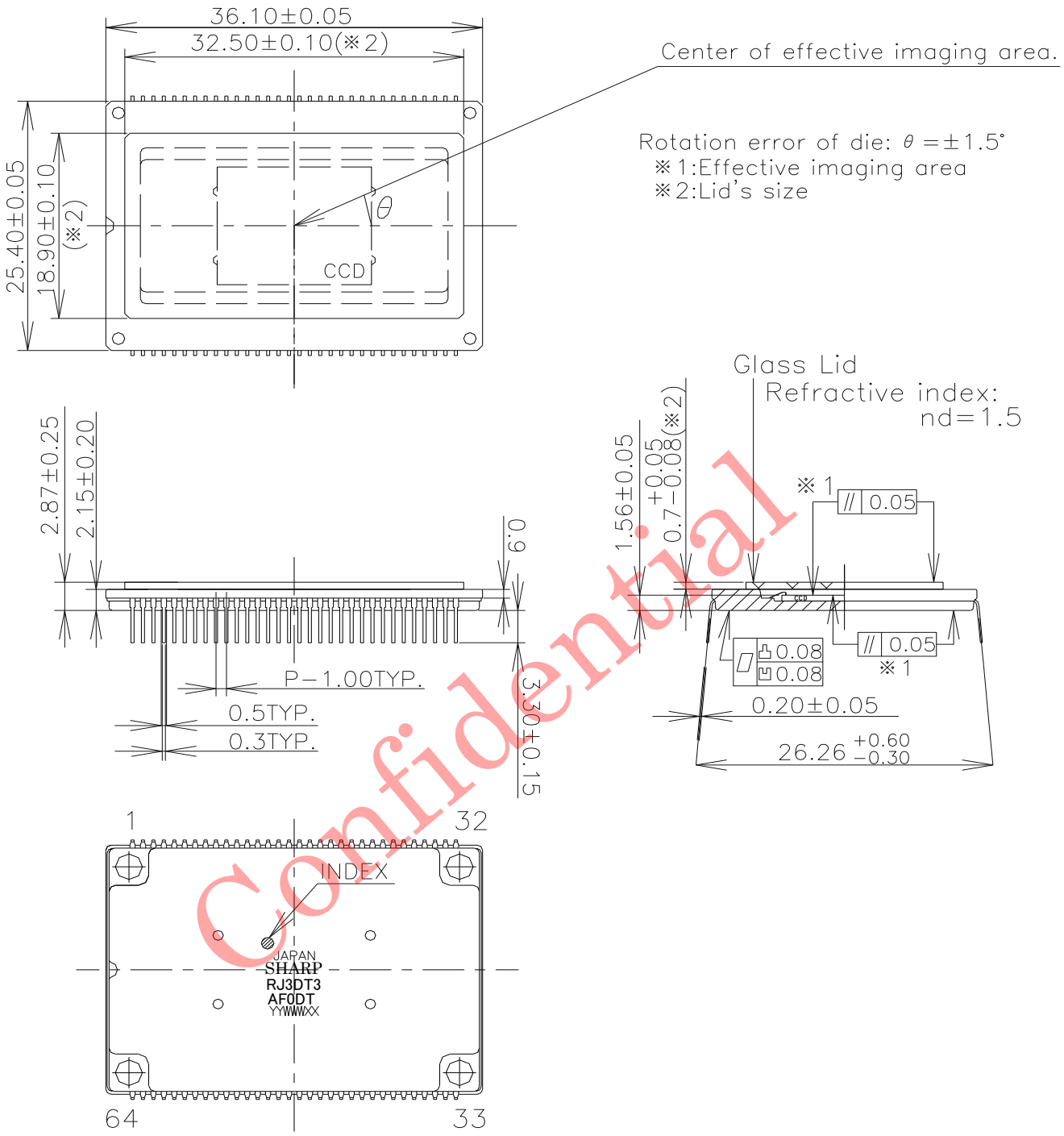
Names and Contents of the Hazardous Substances.

Hazardous Substances					
Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
○	○	○	○	○	○

This table is prepared in accordance with the provisions of SJ/T 11364.

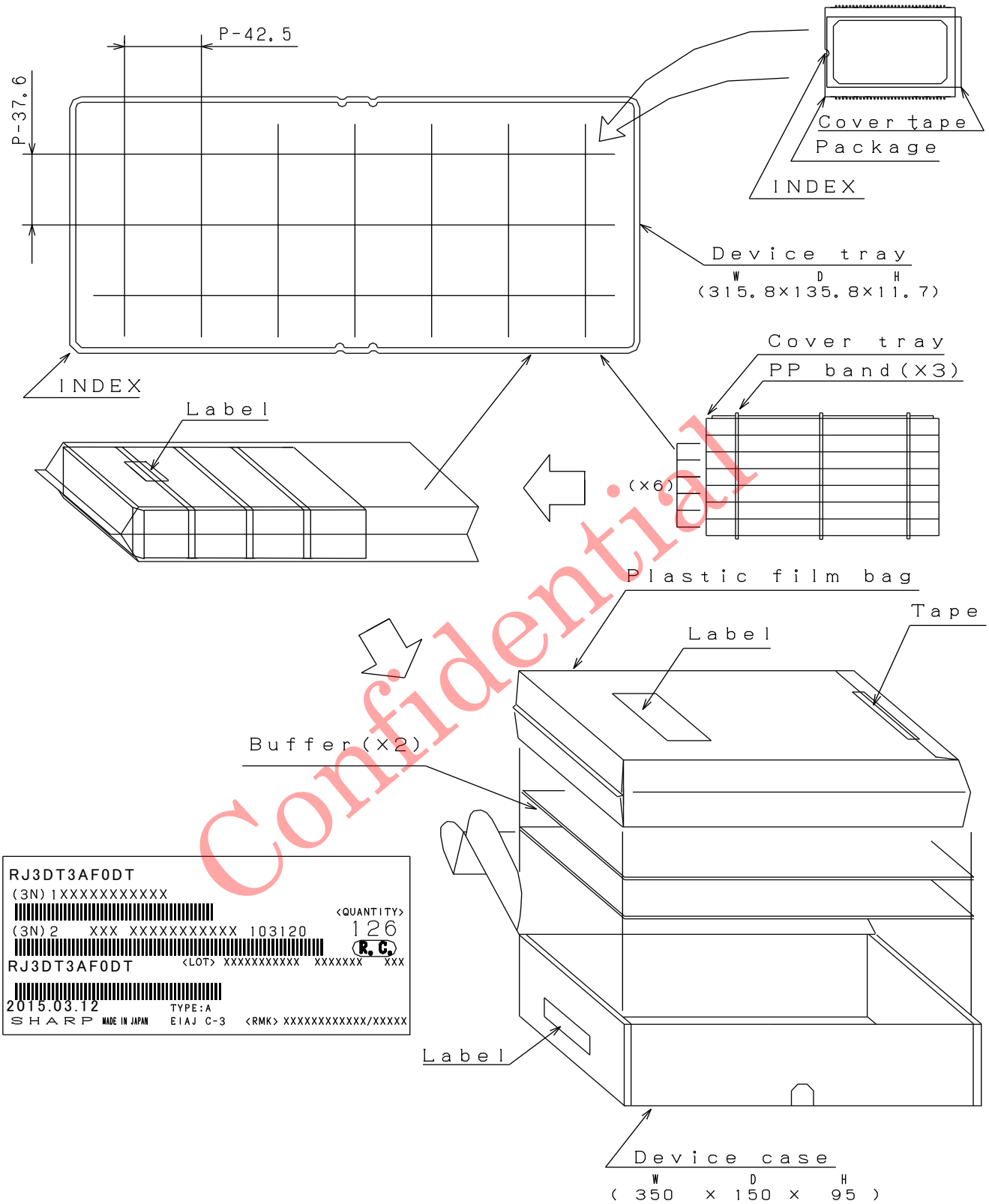
○ : Indicates that said hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement of GB/T 26572.

× : Indicates that said hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement of GB/T 26572.



(UNIT:mm)

材質 MATERIAL	仕上 FINISH	名称 NAME	WDIP64-P-1000 Package Outline Specification
		コード CODE	
Assembly Process Production Engineering Dept. I			
ELECTRONIC COMPONENTS AND DEVICES GROUP		図番 DRAWING No.	GDP064A-15E3
SHARP CORPORATION			



(UNIT:mm)

材質 MATERIAL	仕上 FINISH	名称 NAME	External Appearance of Packing
		コード CODE	
Assembly Process Production Engineering Dept. I			
ELECTRONIC COMPONENTS AND DEVICES GROUP		図番 DRAWING No.	KSEC-126TA-2
SHARP CORPORATION			